

**IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION**

OCEAN SEMICONDUCTOR LLC, <i>Plaintiff,</i> vs. MEDIATEK INC., ET AL., <i>Defendant.</i>	Case No. 6:20-cv-01210-ADA
OCEAN SEMICONDUCTOR LLC, <i>Plaintiff,</i> vs. NVIDIA CORPORATION, <i>Defendant.</i>	Case No. 6:20-cv-01211-ADA
OCEAN SEMICONDUCTOR LLC, <i>Plaintiff,</i> vs. NXP SEMICONDUCTORS NV, ET AL., <i>Defendant.</i>	Case No. 6:20-cv-01212-ADA
OCEAN SEMICONDUCTOR LLC, <i>Plaintiff,</i> vs. RENESAS ELECTRONICS CORPORATION, ET AL., <i>Defendant.</i>	Case No. 6:20-cv-01213-ADA
OCEAN SEMICONDUCTOR LLC, <i>Plaintiff,</i> vs. SILICON LABORATORIES INC., <i>Defendant.</i>	Case No. 6:20-cv-01214-ADA
OCEAN SEMICONDUCTOR LLC, <i>Plaintiff,</i> vs. STMICROELECTRONICS INC., <i>Defendant.</i>	Case No. 6:20-cv-01215-ADA
OCEAN SEMICONDUCTOR LLC, <i>Plaintiff,</i> vs. WESTERN DIGITAL TECHNOLOGIES, INC., <i>Defendant.</i>	Case No. 6:20-cv-01216-ADA

DECLARATION OF COSTAS SPANOS, PH.D.

I, Costas Spanos, Ph.D., declare as follows:

I. INTRODUCTION

1. I have been retained by counsel for Defendants MediaTek Inc.; MediaTek USA Inc.; NVIDIA Corporation; NXP USA, Inc.; Renesas Electronics Corporation; Renesas Electronics America, Inc.; Silicon Laboratories Inc.; STMicroelectronics, Inc.; and Western Digital Technologies, Inc. as an expert to analyze and explain certain claim terms in U.S. Patent Nos. 6,660,651 (“the ’651 patent”), 8,676,538 (“the ’538 patent”), and 6,420,097 (“the ’097 patent”).

2. In rendering my opinions, I considered the items discussed or listed herein, as well as my own experiences in the field of semiconductor manufacturing technology. I have also reviewed the parties’ lists of claim terms for construction as well as the parties’ proposed constructions.

3. I reserve the right to amend or supplement my opinions in light of further documents, depositions, or discovery disclosures.

4. I am being compensated at my usual hourly rate of \$750 and I am being separately reimbursed for any out-of-pocket expenses. My compensation does not depend in any way on the outcome of this case, my particular testimony, or the opinions that I express.

II. QUALIFICATIONS & EXPERIENCE

5. I have attached my Curriculum Vitae as Exhibit 1.

6. I am a Professor of Electrical Engineering and Computer Sciences at the University of California in Berkeley, California.

7. I graduated from the National Technical University of Athens, Greece in 1980 with a five-year diploma in in Electrical Engineering, specialized in Electronics. I then graduated from

Carnegie Mellon University in 1981 with a M.S. in Electrical Engineering, specialized in Computer-Aided Design of Integrated Circuits (ICs), and in 1985 with a Ph.D. in Electrical Engineering, specialized in Computer-Aided Fabrication of ICs.

8. In the course of my professional and academic career, I have taught courses in semiconductor technology and semiconductor manufacturing at both the undergraduate and graduate levels, and I have also presented multiple short courses on the subjects of statistical process control and experimental design in semiconductor manufacturing to industrial audiences.

9. I have published more than 300 peer-reviewed publications on all these subjects and co-authored a well-cited textbook. I have also been involved in co-founding two successful companies. The first, Timbre Technologies, specialized in sub-nm metrology for ultra-fine patterns that need to be produced and controlled during advanced semiconductor processing. The second, OnWafer Technologies, specialized in wireless, in-situ monitoring of critical steps during photolithography and plasma operations. Timbre Technologies was acquired by Tokyo Electron, and OnWafer Technologies was acquired by KLA-Tencor. The technologies Timbre Technologies and OnWafer Technologies were based on are widely in use today across the semiconductor industry.

10. In addition to my academic and commercial work, I have been at times retained as an expert witness in several patent disputes relating to semiconductor manufacturing technology, where I have provided expert opinions and testimony.

III. LEVEL OF ORDINARY SKILL IN THE ART

11. The '651 patent relates to an adjustable wafer stage on which a process operation is performed on a wafer. '651 patent at 1:6-11, 2:26-57, 3:9-14, 5:3-29, 7:28-34. The '538 patent relates to determining a relationship between processing parameters such as temperature or pressure and "faults" (undesired parameter values) detected during processing and adjusting the

weighting of parameters before performing subsequent fault detection algorithms. '538 patent at 1:9-12, 5:28-59.

12. For each of the '651 and '538 patents, a person of ordinary skill in the art at the time of the alleged invention would have had at least a B.S. in mechanical engineering, electrical engineering, materials science engineering, or a related field. A person of ordinary skill in the art at the time of the alleged invention also would have had experience with the technological area relating to the patents at issue. In the case of the '651 patent, in addition to the educational requirement described above, a person of ordinary skill in the art at the time of the alleged invention would have had four years of experience designing and developing semiconductor fabrication processes and tooling. For the '538 patent, in addition to the educational requirement described above, a person of ordinary skill in the art at the time of the alleged invention would have had four years of experience working with semiconductor fabrication processes, including computer programming and data analysis. If someone had an M.S. or Ph.D. in mechanical engineering, electrical engineering, materials science engineering, or a related field, then less experience would have been necessary to qualify that person as a person of ordinary skill in the art at the time of the alleged invention for each of the '651, and '538 patents.

13. The '097 patent relates to trimming or reducing the linewidth of a hardmask layer in a semiconductor film stack in order to achieve linewidths of circuit structures (like transistor gates), formed using a hardmask, that are narrower than the linewidths generated by conventional lithography tools at the time of the alleged invention. '097 patent at 1:4-9, 1:57-63.

14. For the '097 patent, a person of ordinary skill in the art at the time of the alleged invention would have had a B.S. in chemical engineering, materials science, electrical engineering, physics, chemistry, or a similar field, and three or four years of work experience in integrated

circuit fabrication or related fields. If someone had an M.S. or Ph.D. in chemical engineering, materials science, electrical engineering, physics, chemistry, or a similar field, then less experience would have been necessary to qualify that person as a person of ordinary skill in the art at the time of the alleged invention for purposes of the '097 patent.

15. I meet the qualifications of a person of ordinary skill in the art for each of the '651, '538, and '097 patents. I have a Ph.D. in Electrical Engineering and several years of experience researching issues and developing solutions in each of the technology areas relating to the patents at issues.

IV. LEGAL STANDARDS

A. Claim Construction

16. I am informed on the law regarding claim construction and patent claims, and understand that a patent may include two types of claims, independent claims and dependent claims. An independent claim stands alone and includes only the limitations it recites. A dependent claim can depend on an independent claim or another dependent claim. I understand that a dependent claim includes all the limitations that it recites in addition to all the limitations recited in the claim or claims from which it depends.

17. I understand that claim construction is a matter of law for the Court to decide. Claim terms should be given their ordinary and customary meaning within the context of the patent in which the terms are used, *i.e.*, the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention in light of what the patent teaches.

18. I understand that to determine how a person of ordinary skill would understand a claim term, one should look to those sources available that show what a person of skill in the art would have understood disputed claim language to mean. Such sources include the words of the claims themselves, the remainder of the patent's specification, the prosecution history of the patent

and the cited references (all considered “intrinsic” evidence), and “extrinsic” evidence, such as dictionary definitions and learned treatises and the opinions of qualified experts concerning relevant scientific principles, the meaning of technical terms, and the state of the art.

19. I understand that, in construing a claim term, one looks primarily to the intrinsic patent evidence, including the words of the claims themselves, the remainder of the patent specification, and the prosecution history.

20. I understand that extrinsic evidence, which is evidence external to the patent and the prosecution history, may also be useful in interpreting patent claims.

21. I understand that words or terms should be given their ordinary and accepted meaning unless it appears that the inventors were using them to mean something else. In making this determination, the claims, the patent specification, and the prosecution history are of paramount importance. Additionally, the specification and prosecution history must be consulted to confirm whether the patentee has acted as its own lexicographer (i.e., provided its own special meaning to any disputed terms), or intentionally disclaimed, disavowed, or surrendered any claim scope.

22. I understand that a person of ordinary skill in the art is deemed to read a claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification. For this reason, the words of the claim must be interpreted in view of the entire specification. The specification is the primary basis for construing the claims and provides a safeguard such that correct constructions closely align with the specification. Ultimately, the interpretation to be given a term can only be determined and confirmed with a full understanding of what the inventors actually invented and intended to envelop with the claim as set forth in the patent itself.

B. Indefiniteness

23. I understand that a patent must satisfy a definiteness requirement, which requires that it conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as the invention.

24. I understand that definiteness requires that a patent's claims, viewed in light of the specification and file history from the perspective of a person skilled in the relevant art, inform those skilled in the art about the scope of the invention with reasonable certainty.

25. I understand that patents are presumed valid and indefiniteness is an invalidity defense. So, I understand that indefiniteness must be shown by clear and convincing evidence.

V. "A SIGNIFICANT FAULT" ('538 PATENT CLAIM 5)

Term	Ocean's Construction	Defendant's Construction
"A significant fault" ('538 Patent, Claim 5)	No construction is necessary, or in the alternative, "abnormality or fault that relates to an actual fault."	Indefinite

26. In my opinion, the claim limitation that uses the term "a significant fault" to describe whether a "detected fault" is "a significant fault" in the '538 patent is indefinite. A person of ordinary skill would not be able to understand the scope of those claim limitations with reasonable certainty.

27. Claim 5 of the '538 patent uses the term "a significant fault" to describe a "detected fault." "5. The method of claim 1, further comprising: designated in said computer whether said detected fault is *a significant fault*; and adjusting said weighting associated with said parameter based responsive to designating said detected fault as *a significant fault*." A POSITA would not be able to understand the scope of this limitation with reasonable certainty. In this field and in the context of the patent and claims, it is impossible to know how far a fault must deviate from its

expected value to be “significant,” or how out of specification a workpiece must be before experiencing a “significant” fault. In other words, it is unclear how far a fault could deviate from its expected value to be an insignificant or normal fault, or how out of specification a workpiece could be and still be experiencing only an insignificant or normal fault. Nothing in the claims or specification of the patent provides any guidance to a POSITA to make this determination and thus understand the boundaries of this term. In my opinion, it would be purely subjective, and depend on, for example, the manufacturing tools, the products being manufactured, the level of precision required by the designer and fabricator, among many other potential factors.

28. I have reviewed the patent and did not find any disclosure that provides a definition, parameters, or other metrics to determine the boundaries of what is or isn’t “significant.” The specification only explains that “[t]he system 300 analyzes the fault data resulting from the fault data analysis and/or the PCA, in order to determine whether any particular parameters associated with any faults or abnormalities detected that are associated with the processing of semiconductor wafers 105 is actually a significant fault.” ’538 patent at 11:12-19. There is no disclosure in the patent for how to make that determination, however.

29. The other example of the word “significant” being used in the specification (at 11:29-67) is not related to determining whether a fault is “significant.” Instead, it discusses that certain parameters may be a “significant contribution” to a fault. The disclosure does not provide a way to determine what is (or isn’t) “significant.” See also ’538 patent at Fig. 8.

30. A POSITA also would not understand the bounds of the claims because the word “significant,” without additional explanation, is a subjective word of degree and it does not indicate any specific amount, range, or parameter to me. It is an inexact term I would never use if I had to describe a value in this field with reasonable certainty. I do not know, for example, if these claims

would cover a situation where a fault is 5% out of specification, or if it would only cover a situation where a fault is 10% out of specification, or a situation where a fault is 15% out of specification. Whether a fault is “significant” may depend on numerous factors not disclosed by the ‘538 patent. For example, two engineers may disagree whether a “fault” is “significant” due to, e.g., the subjective demands of their customers (e.g., the variance permitted by a customer) or the material used in the manufacturing process (e.g., some materials are more fault tolerant). A POSITA is thus left guessing what qualifies as a “significant” fault in this claim. As such, it is my opinion that a POSITA would not know the outer bounds of what is being claimed with reasonable certainty.

31. I also do not agree with Plaintiff’s construction for this term. It does not provide any actual definition and only imports more ambiguity into the term. Rather than provide a construction that defines how much a fault must be out of specification to be a significant fault, Plaintiff instead proposes a construction that redefines the term using unclear concepts such as “abnormality” and undefined terms like “relates to an actual fault.” If Plaintiff’s alternative construction were to be adopted, it too would fail to inform a POSITA of the bounds of the claim because a POSITA would not understand what is meant by “fault relat[ing] to an actual fault.” Moreover, what qualifies as an “actual fault” is itself subjective and dependent on external factors. For example, the exact same fault may be an “actual fault” if the result falls outside the scope of an acceptable variance defined by customer A, but may not be an “actual fault” if customer B has a wider definition of acceptable variance.

VI. “DETERMINING IN SAID COMPUTER WHETHER SAID PARAMETER IS A SIGNIFICANT FACTOR” (’538 PATENT, CLAIM 7)

Term	Ocean’s Construction	Defendant’s Construction
“determining in said computer whether said parameter is a	No construction is necessary, or in the alternative, “a	Indefinite

significant factor” (’538 Patent, Claim 7)	parameter that provides a significant contribution to the fault.”	
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32. In my opinion, the claim limitation that uses the term “a significant factor” to describe whether the “parameter” “provides a significant contribution” in the ’538 patent is indefinite. A person of ordinary skill would not be able to understand the scope of those claim limitations with reasonable certainty.

33. Claim 7 of the ’538 patent uses the term “a significant factor” to describe a “parameter”: “7. The method of claim 1, wherein determining in said computer said relationship of a parameter relating to said fault detection analysis to a detected fault further comprises determining in said computer whether said parameter is *a significant factor* associated with said fault.”

34. A POSITA would consider this term indefinite because, in this field and in view of the patent and its claims, it is impossible to know what would it take to make a “parameter” a “significant contribution associated with [a] fault.” Nothing in the claims or specification of the patent provides any guidance. When the term is used in the specification, the specification does not provide a definition or any objective boundaries as to the term’s meaning. The specification states: “The system 300 may also comprise a dynamic PCA weighting module 370, which is capable of receiving data automatically and/or manually relating to information indicating whether a particular parameter that was considered abnormal is indeed a significant factor in any detected faults.” ’538 patent at 7:36–40. There are no metrics, parameters, or even characteristics from the specification that a POSITA could rely on to understand the boundaries of the term.

35. Further, a POSITA would not understand the boundaries of the claims with reasonable certainty because the word “significant” is a subjective word of degree and it does not

indicate a specific amount, parameter, or metric. For example, there is no indication if the claims would cover a parameter where it is 10% responsible for contributing to a fault, or if it would only cover a parameter where it is 25% responsible for contributing to a fault, or if it would only cover a parameter where it is 50% responsible for contributing to a fault. Whether a parameter is a “significant factor” in a fault may depend on numerous factors not disclosed by the ‘538 patent. For example, two engineers may disagree whether a “factor” is “significant” due to the presence of additional factors that may appear to also be significant. It is an inexact term I would never use if I had to clearly describe a value in this field with reasonable certainty. Thus, it is my opinion that a POSITA cannot know the outer bounds of what is being claimed in this claim with reasonable certainty.

36. I also do not agree with Plaintiff’s construction for this term. It does not provide any actual definition and only imports more ambiguity into the term. Rather than attempt to provide a construction that defines how closely linked to a fault a parameter must be in order to be deemed “significant,” Plaintiff instead proposes a construction that merely replaces the indefinite “a significant factor” with the equally indefinite “a significant contribution.” What qualifies as “a significant contribution” is itself subjective given the continued use of “significant.” The alternative construction still renders it impossible for a POSITA to know the bounds of the claim.

VII. “PNEUMATIC CYLINDER” (’651 PATENT, CLAIMS 19, 75, 81)

Term	Ocean’s Construction	Defendant’s Construction
“pneumatic cylinder” (’651 Patent, Claims 19, 75, 81)	No construction is necessary, or in the alternative, “a pneumatic, hydraulic, electromagnetic or mechanical device”	Plain and ordinary meaning

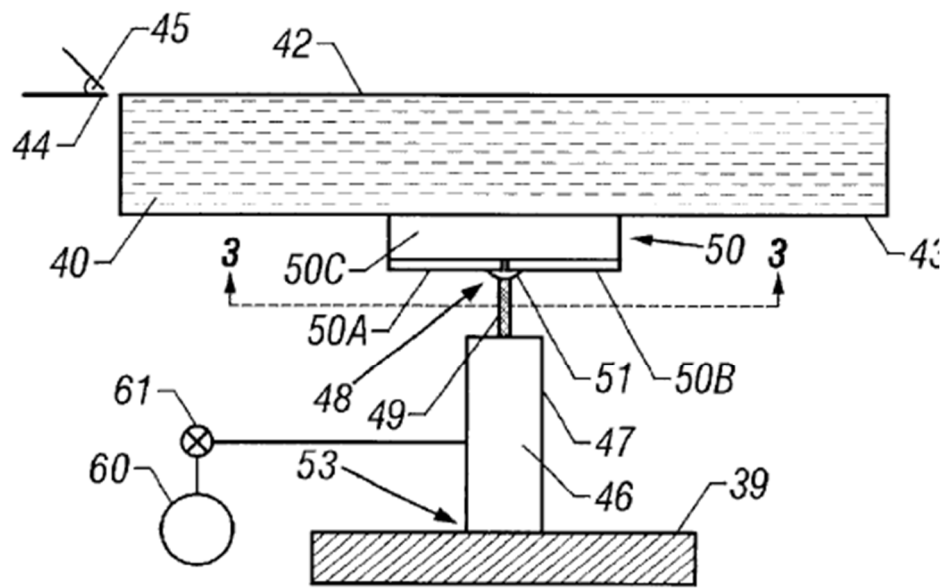
37. In my opinion, the claim limitation “pneumatic cylinder” as used in the ’651 patent should be given a construction consistent with its plain and ordinary meaning.

38. The ’651 patent describes different types of mechanisms for “adjusting the position of the wafer stage,” including “pneumatic, hydraulic, electromagnetic, or mechanical systems.” ’651 patent at 5:65–6:1.

39. A POSITA, consistent with the ’651 patent specification, would have understood these to be four different types of devices—all included in Ocean’s construction for pneumatic—that have different ways of causing movement in order to move the wafer stage.

40. A pneumatic device is a device that is powered by compressed air or other gas. “Pneumatic,” means that the power to actuate the device is generated by air or other gas pressure. *See* American Heritage Dictionary published 2001, reissued 2004 (“Of or relating to air or other gases” or “Filled or operated by air”); Dictionary of Engineering 1997 (“Pertaining to or operated by air or other gas”); Merriam-Webster Dictionary 2001 (“of, relating to or using gas (as air or wind)” and “moved or worked by air pressure”); ’651 patent at 6:1–21.

41. One specific type of a pneumatic device is a pneumatic cylinder, which is a cylindrical device that uses pressurized air or other gas to move a shaft (or rod) of the device along a linear path (that is, in a straight line). A pneumatic cylinder is described in the ’651 patent and in the literature known to a POSITA. ’651 patent at 6:1–65, Figure 2 (reproduced below, depicting “pneumatic cylinder 46 ... comprised of a housing 47 [and] a shaft 49” where pressurized air or an inert gas is supplied to the cylinder to move its shaft 49 in a linear direction), Figure 3; Pneumatic Systems at 85 (“Pneumatic cylinders offer a straight rectilinear motion to mechanical elements.”), 85 (“The pneumatic power is converted to straight line reciprocation motions by pneumatic cylinders”), 86–89.

**FIG. 2**

42. As the '651 patent notes, in describing the pneumatic cylinders 46 of Figure 2, "The pneumatic cylinders 46 may be any type of pneumatic cylinders useful for performing the function of adjusting the surface 42 of the wafer stage 40. For example, the pneumatic cylinders 46 may be dual-acting pneumatic cylinders. The stroke, size and supply pressure to such cylinders may vary depending upon the particular application. Air or inert gas may be supplied to the cylinders 46 at the required pressure through flexible houses (not shown)." '651 patent at 6:13–21. The Pneumatic Systems book further describes such a dual (double) acting pneumatic cylinder. Pneumatic Systems at 89.

43. As evidenced by the patent and other literature understood to a POSITA, the critical feature of pneumatic devices is that they are powered by air or other gas pressure.

44. The other types of devices—consistent with their names—are powered by particular means (hydraulic, electromagnetic, and mechanical forces, respectively). More particularly, the second type of device mentioned in the '651 patent is a hydraulic device, which,

as the “hydraulic” in its name demonstrates, is a device powered by pressurized liquid fluids. The third type, an electromagnetic device, is powered by an electric current and a magnetic field. And the fourth type, a mechanical device, is a device that creates the needed motion through interacting mechanical parts, as, for example, in a rack and pinion configuration.

VIII. “ULTRA-THIN RESIST LAYER” (’097 PATENT, CLAIMS 1-3, 10-17)

Term	Ocean’s Construction	Defendant’s Construction
“ultra-thin resist layer” (’097 Patent, Claims 1-3, 10-17)	No construction is necessary.	Indefinite

45. I have been asked to opine as to what a person of skill in the art at the time of the invention (POSITA) would have understood by the claim term “ultra-thin resist layer[s]” and whether a POSITA would have understood, based on the claims, specification, prosecution history, and extrinsic evidence, whether “ultra-thin resist layer[s]” has a defined upper limit and if so, what that upper limit is. In this declaration, I use UTR to refer to “ultra-thin resist” and UTR layer to refer to “ultra-thin resist layer[s].”

46. The ’097 patent describes a method for forming circuit structures having linewidths smaller than conventional lithography techniques allowed. ’097 patent at 1:4–9. Lithography uses light of specific wavelengths to expose and generate linewidth patterns in a layer of photoresist material. ’097 patent at 1:16–20. The patterned photoresist is used as a sacrificial layer in the way of creating circuit structures, such as gates, from underlying layers. ’097 patent at 1:60–63, 4:14–42.

47. The ’097 patent teaches forming the stack of layers shown in Figure 4(b) (see below) that includes substrate 114, device layer 116, hardmask layer 118, and UTR layer 120 (shaded blue). ’097 patent at 3:63–4:2. Figure 4(c) below shows that UTR layer 120 is then patterned to form resist mask 122 (shaded blue). Resist mask 122 is further processed to create a

device structure such as a transistor gate with a linewidth narrower than the original width of the resist mask. '097 patent at 4:14–42.



48. The term “ultra-thin resist layer[s]” (UTR layer) appears explicitly in only claims 1 and 4. '097 patent at 5:34-35, 5:40-41 (claim 1), 6:7 (claim 4). Without consulting the specification, prosecution history, or extrinsic evidence, a POSITA would have understood that “resist layer” refers to a layer of photoresist and further that “ultra-thin” modifies “resist layer,” so that UTR layer refers to resist layers having thicknesses that would have been considered very thin at the time of the invention. The resist layer’s thickness is the characteristic that qualifies it as “ultra-thin,” which is a term of degree for thickness. That is, UTR layer refers to resist layers having thicknesses that fall within a certain range of thicknesses. However, a POSITA would not have known the limits of that thickness range based on the term alone. In fact, the term UTR layer begs the question as to what range of thicknesses qualifies as a UTR layer in the context of the alleged invention.

49. The claims of the '097 patent support my opinion that UTR layer corresponds to resist layers having thicknesses that fall within a certain range, given the intended application. Claim 1 does not specify any resist thicknesses. However, claim 4 recites “[a] method of forming circuit structures as claimed in claim 1, wherein the *ultra-thin resist layer has a thickness of less than 2500 Å*” (emphasis added). The language of claim 4 makes clear that for purposes of claim

4 (and claims 5-9, which refer back to claim 4 directly or through an intermediate claim), the UTR layer must have a thickness of less than 2500 Å. That is, a POSITA would understand claim 4 specifies a range of thicknesses for resist layers that qualify as a UTR layer: less than 2500 Å.

50. Because claim 4 depends on claim 1 and includes a limitation on UTR layer not found in claim 1 (the range of “less than 2500 Å”), a POSITA would have understood that the thickness range of UTR layer in claim 1 (and claims 2–3 and 10–17, which refer back to claim 1 directly or through an intermediate claim) has an upper limit **greater** than “less than 2500 Å,” that is, an upper limit of 2500 Å or greater. But this again begs the question: what range of thicknesses qualifies as a UTR layer in claims 1-3 and 10-17? A POSITA would have understood that the language of claim 1, considered in light of the language of claim 4, indicates not what the upper limit of UTR layer thickness is, but what it is not—“less than 2500 Å.”

51. Likewise, the specification of the '097 patent does not specify an upper limit for UTR layer thickness. The '097 patent states that “a resist coating having an UTR thickness is considered to be resist films of less than 0.25 μm (2500 Å) in thickness” ('097 patent at 1:43–45) and describes the problem associated with the prior art approach when applied to “an ultra-thin resist thickness of less than 2500 Å” ('097 patent at 2:32-34 (“FIGS. 2(a)-2(d) illustrate the problem of applying the conventional lithographic process of FIGS. 1(a)-1(d) to an UTR having a thickness of less than 2500 Å”), 2:58-61 (“Further, the problem associated when the conventional lithographic process is applied to an ultra-thin resist thickness of less than 2500 Å will also be explained in connection with FIGS. 2(a) through 2(d).”), 3:33-40 (“However, when the lithographic process described above in FIGS. 1(a)-1(d) is applied to an UTR thickness of less than 2500 Å, there is created a significant problem in the gate conductor etching process since an excessive amount of resist will have been consumed during the trim process step. As can be seen

in FIG. 2(a), an UTR layer 18a has a thickness of less than 2500 Å as compared to the thicker resist layer 18 of FIG. 1(a).”), Fig. 2a). Similarly, the only thickness associated with UTR layer in the description of the embodiments of the invention is “less than 2500 Å.” ’097 patent at 4:12-13 (“UTR layer 120 has a thickness of less than 2500 Å”), Fig. 3 (step 304, “Deposit resist layer of less than 2500 Å over hardmask”). These disclosures establish that resist films with thicknesses under 2500 Å qualify as UTR layers. They do not, however, establish the upper limit of the thickness of UTR layers.

52. The ’097 patent’s discussion of thicknesses other than “less than 2500 Å” also does not establish the upper limit of the thickness of UTR layer. The patent describes a “standard” resist thickness of 5000 Å or more for 248 nm lithography and of 4000 Å for 193 nm lithography.¹ ’097 patent at 1:39–43 (“In the current state-of-the-art, integrated circuit manufacturers have been using in the resist process a resist coating having a standard photoresist thickness of more than 0.5 μm (5,000 Å) for 248 nm lithography and 0.4 μm (4,000 Å) for 193 nm lithography.”), 2:29–31 (“FIGS. 1(a)-1(d) illustrate cross-sectional views of a conventional lithographic process utilizing a standard resist having a thickness of about 5000 Å”), 2:51–58 (“Before describing in detail the improved method... first explaining the conventional lithographic process used on a standard resist having a thickness of about 5000 Å for forming a gate conductor with reference to FIGS. 1(a) through 1(d).”), 3:2–3 (“The resist layer has a thickness of approximately 5000 Å in the current art.”), Fig. 1a. Thus, the patent discloses that the “standard” resist thickness varies depending on the wavelength of light used during a lithography process: the standard resist thickness is larger for 248 nm lithography (5000 Å or more) than it is for 193 nm lithography (4000 Å). ’097 patent

¹ The figures of 248 nm and 193 nm refer to the wavelengths of light used for patterning photoresist.

at 1:39–43, 2:29–31, 2:51–58, 3:2–3, Fig. 1a. These disclosures are consistent with the knowledge of a POSITA, namely that the absorption of light by a photoresist increases as the wavelength used for photolithography decreases, such that thinner photoresist layers are used at shorter wavelengths. The disclosures and the related understanding about photoresist thickness as a function of lithography wavelength would have suggested to a POSITA that the thickness range for UTR layer also varies based on the type of lithography being used.

53. The specification does not address what thicknesses between 2500 Å and 5000 Å for 248 nm lithography or between 2500 Å and 4000 Å for 193 nm lithography qualify as “ultra-thin.” That is, the specification does not identify the thickness between 2500 Å and 5000 Å that is the upper limit of UTR layer for 248 nm lithography nor the thickness between 2500 Å and 4000 Å that is the upper limit of UTR layer for 193 nm lithography. Thus, the specification, like the claims, does not tell a POSITA the upper limit for thickness of the UTR layer recited in claims 1–3 and 10–17.

54. I reviewed the prosecution history of the '097 patent and found it did not provide any information beyond that provided in the specification and claims as to the upper limit of thickness of UTR layer.

55. Extrinsic evidence does not provide information—missing from the claims, specification, and prosecution history—that removes the uncertainty as to the upper limit of thickness of UTR layer. For example, a POSITA would have been aware that several patents filed shortly before the '097 patent (filed May 2, 2000) and originally assigned, like the '097 patent, to Advanced Micro Devices, Inc. (AMD), use the term UTR layer or a variant such as “ultra-thin photoresist.” Five such patents that list as an inventor Scott A. Bell, co-inventor of the '097 patent, disclosed an “ultra-thin photoresist layer” with “a thickness of about 500 Å-5000 Å.” U.S. Patent

No. 6,127,070 at 7:19–20; U.S. Patent No. 6,140,023 at 6:15–16; U.S. Patent No. 6,309,926 at 8:34–35; U.S. Patent No. 6,162,587 at 7:22–23; U.S. Patent No. 6,165,695 at 7:31–32. A sixth patent filed a day before the '097 patent describes that “[u]ltra-thin photoresists . . . have a thickness of about 3,000 Å or less.” U.S. Patent No. 6,451,512 at 3:49–50. A seventh patent filed in June 1999 identifies an upper limit for UTR layer thickness that corresponds to yet another value—“about 2500 Å.” U.S. Patent No. 6,156,480 at 3:44–46.

56. Other contemporaneous patents assigned to AMD explain that “[u]ltra-thin resists . . . have a thickness of about 5,000 Å or less.” U.S. Patent No. 6,762,133 at 4:4–5; U.S. Patent No. 6,645,702 at 3:62–64. An additional patent assigned to AMD describes an “ultra thin photoresist layer having a thickness from about 2,000 angstroms to about 5,000 angstroms.” U.S. Patent No. 6,746,973 at 12:55–59. These three patents were filed between July 2001 and August 2002, shortly after the May 2, 2000 filing of the '097 patent.

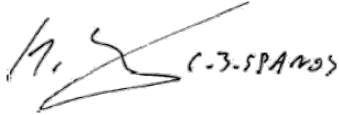
57. Other contemporaneous patents listing as an inventor one of the two co-inventors of the '097 patent identify an upper limit for UTR thickness of 2500 Å. U.S. Patent No. 6,566,214 at 3:49–52 (“2500 Angstroms or less”); U.S. Patent No. 6,326,319 at 1:47–50 (“2,500 Å or less”). Scott A. Bell is listed as an inventor of the former patent. Christopher L. Pike is listed as an inventor of the latter patent. These patents were filed between July 2000 and January 2002.

58. The extrinsic evidence discussed above confirms that at the time of the invention, the upper limit on the thickness of UTR could have been one of several different values, such as 5000 Å, 3000 Å, or 2500 Å. Thus, the upper limit on the thickness of UTR was not a well-defined quantity in the art. As a result, a POSITA encountering the term UTR layer would have been obliged to seek a specific teaching within the disclosure to determine its upper limit. However, nothing in the '097 patent claims, specification, or prosecution history provides that specific

teaching. Accordingly, a POSITA would have been unable to determine the upper limit of thickness for the term UTR layer in claims 1-3 and 10-17.

I declare under penalty of perjury that the foregoing is true and correct. Executed on October 6, 2021.

SIGNATURE

A handwritten signature in black ink, appearing to read "C. J. Spanos", written over a horizontal line.

Costas J. Spanos

EXHIBIT 1

Costas J. Spanos
Andrew S. Grove Distinguished Professor
Electrical Engineering and Computer Sciences
University of California, Berkeley CA 94720-1770
spanos@berkeley.edu, 510 643 6776

Professional History

- **Department of EECS**

Jul 95 – present Professor of Electrical Engineering and Computer Sciences

Jul 91 - Jun 95 Associate Professor of Electrical Engineering and Computer Sciences

Jul 88 - Jun 91 Assistant Professor of Electrical Engineering and Computer Sciences

- Specializing in Computer-Aided Manufacturing systems and Design for Manufacturing applications for Integrated Circuits. Founding co-PI of multi-investigator, multi-campus centers, supported by multiple companies and the state of California. PI or co-PI on several industrially funded research projects.
- Specializing in Energy Efficiency. Founding Principal Investigator of multinational, multidisciplinary project on energy efficient buildings including University of California Berkeley, Nanyang Technological University and National University of Singapore, funded by Singapore's National Research Foundation.
- **Director, Center for Information Technology Research in the Interest of Society & the Banatao Institute since 2014**
 - The Center for Information Technology Research in the Interest of Society (CITRIS) was formed in 2001, when researchers within the UC system realized that the real opportunities lay not just in *developing* new and innovative technologies, but also in *applying* them towards societal goals.
 - CITRIS was established to address the most pressing social and environmental issues facing California. To meet this goal, we presently focus our research on several core efforts including Sustainable Infrastructures, Health, People & Robots, the Policy Lab, the Future of Work, and the Women in Tech initiative.
- **Associate Dean for Strategic Initiatives, College of Engineering, 2013 – 2014**
 - Oversaw the College's international collaborations including Singapore, China, and the Philippines, while exploring new prospects in places such as Brazil and Mexico.
 - Joint research programs, opportunities for COE and UCB to participate and lead the development of novel initiatives, and opportunities for our faculty to engage in targeted executive education programs.
- **Founding Director & CEO, Berkeley Educational Alliance for Research in Singapore, 2011 – 2014, 2018 – present**
- **CTO, Berkeley Educational Alliance for Research in Singapore 2014 - 2018**
 - BEARS is the umbrella organization that manages UC's large research programs in Singapore on Energy, which has secured over \$120M in funding.
 - As its founding Director, oversaw built out and operations, including the interaction with the BEARS Governing Board and Singapore's National Research Foundation.

- Leading a broad outreach effort for both corporate and institutional relationships in Singapore and worldwide.
- **EECS Department Chair, 2010- 2012**
 - Oversaw academic personnel, outreach and overall functions and operations for the largest academic department at the University of CA, Berkeley. (85 Regular faculty, 530 graduate students, 1, 200 undergraduate students, ~100M annual research budget. The EECS Department has been consistently rated within the top 3 worldwide in all of our graduate and undergraduate programs.
 - Handled major reorganization in view of dramatically changing CA state budgets.
 - Attracted a major donation by Texas Instruments for the improvement of Cory Hall.
- **EECS Associate Chair, Chair of the EE Division, 2008 – 2010**
 - Oversaw academic personnel actions within the Electrical Engineering Division the EECS Department, worked with Dept. Chair (Professor Stuart Russell) in overall department outreach, strategy and operations.
- **Associate Dean for Research in the College of Engineering, 2004 –2008**
 - Oversaw the ~150M/year Research Enterprise in the College of Engineering.
 - Reorganized four Organized Research Units into the Engineering Research Support Organization (ERSO), recruited its senior leadership and oversaw its operation. ERSO employed about 100 staff and handled the research grants within the College of Engineering. It has now grown into a major Shared-Services unit and is the model for the new “regional” redevelopment across campus. (<http://www.erso.berkeley.edu/>)
 - Drove large programmatic development projects bringing together various faculty constituencies and potential sponsors.
 - Managed matching funds for developing research proposals in strategic areas.
 - Led the effort to streamline industrial support across the College.
 - Participated in numerous campus initiatives relating to research support policies and infrastructure (i.e. Academic Senate Task Force on Industrial Support, Campus Technology Council, Committee to streamline interaction between Berkeley campus and Lawrence Berkeley Laboratory, etc.).
- **Other Appointments**
 - Co-chief Scientist, C3.ai Digital Transformation institute since April 2020.
 - Berkeley Lead, Siebel Energy Institute, 2015-2020.
 - Advisor to Intellectual Ventures on international development projects in Energy Infrastructure, 2013-2014.
 - Program Committee, SPIE conference in Advanced Lithography, 2012- 2014.
 - Advisor to KLA-Tencor on Wireless Metrology, 2007-2014.
 - Intellectual Property Expert for Spansion Japan and Spansion US, 2010.
 - Trade Secret Expert for Taiwan Semiconductor Manufacturing Corporation, 2009.

- Advisor to the United Nations Development Programme on the Sustainable Growth Strategy for the Southeast Anatolia Region, Turkey, 2009-2010.
- Advisor to the Energy Free Home Challenge for the Siebel Foundation 2007-2009.
- Co-Founder, and CEO, OnWafer Technologies (2000-2002), Chief Technology Advisor and Chairman (2003-2007) until OnWafer's acquisition by KLA-Tencor.
- Co-Inventor and Technology Advisor, Timbre Tech (1999-2001), until acquisition by Tokyo Electron.
- Member of the Technical Advisory Board, PDF Solutions.
- Director of the Electronics Research Laboratory 2004 - 2005.
- Intellectual Property Expert for Texas Instruments 1998-2000.
- Founding PI, multi-campus "Small Feature Reproducibility" project 1998- 2003.
- Director of the Berkeley Microfabrication Laboratory 1993-2000.
- Editor of the IEEE Journal "Transactions on Semiconductor Manufacturing" 1991-1994.
- Principal Software Engineer, Digital equipment Corporation 1987-1988
- Senior Software Engineer, Digital equipment Corporation 1985-1987

Education

- May 85, Ph.D. in Electrical Engineering, specialized in Computer-Aided Fabrication of ICs. Carnegie Mellon University, Pittsburgh, PA.
Thesis subject: Statistical IC Process Characterization.
Thesis advisor: Professor S. W. Director.
- July 81, M.S. in Electrical Engineering, specialized in Computer-Aided Design of ICs. Carnegie Mellon University, Pittsburgh, PA.
Thesis subject: Techniques for bi-Objective Decision Making.
Thesis advisor: Professor S. W. Director.
- June 80, Diploma (5 years) in Electrical Engineering, specialized in Electronics. National Technical University of Athens, Greece.
Thesis subject: Hybrid Computer Communication Protocols.
Thesis advisor: Professor E. N. Protonotarios

Honors, Awards

- 1977 and 1979 Greek Institute of State Scholarships Awards.
- 1992 International Semiconductor Manufacturing Science Symposium Best Paper Award
- 1997, 2001, 2005, 2007 IEEE Transactions in Semiconductor Manufacturing Best Paper Awards
- 2008 AEC/APC Best student paper award (with Jing Xue).
- 2013 CASE Best application paper award (with Kevin Weekly).
- 2015 UBICOMM Best paper award (with Ming Jin).
- Fellow of the IEEE, class of 2000.
- Holder of the Andrew S. Grove Distinguished Professorship in EECS since 2009.
- 2016 UC Berkeley Graduate Assembly Faculty Mentor Award.
- 2018 Building and Environment Best Paper Award.

Textbook

Fundamentals of Semiconductor Manufacturing and Process Control” by [Gary S. May](#) and [Costas J. Spanos](#), Wiley Interscience, 2006.

Refereed Journal Publications

1. Costas J. Spanos and S. W. Director, “Parameter Extraction for Statistical IC Process Characterization”, IEEE Trans. on CAD Vol. CAD-5 No 1, pp. 66-79, January 1986
2. Costas J. Spanos, “Statistical Significance of Error-Corrupted IC Measurements”, IEEE Trans. on Semiconductor Manufacturing Vol. 2 No 1, pp. 23-27, February 1989.
3. K. K. Lin and Costas J. Spanos, “Statistical Equipment Modeling for VLSI Manufacturing: An Application for LPCVD”, IEEE Trans. on Semiconductor Manufacturing Vol. 3, No 4, pp. 216-30, November 1990.
4. N. H. Chang and Costas J. Spanos, “Continuous Equipment Diagnosis Using Evidence Integration: An Application for LPCVD”, IEEE Trans. on Semiconductor Manufacturing Vol. 4 No 1, pp. 43-51, February 1991.
5. G.S. May, Costas J. Spanos and J. Huang, “Statistical Experimental Design in Plasma Etch Modeling”, IEEE Trans. on Semiconductor Manufacturing Vol-4 No 2, pp. 83-99, May 1991.
6. Costas J. Spanos, “Statistical Process Control in Semiconductor Manufacturing”, Proceedings of the IEEE, Vol. 80, No. 6, pp. 819-30, June 1992.
7. Costas J. Spanos, Haifang Guo, Alan Miller and Joanne Levine-Parrill, “Real-Time Statistical Process Control Using Tool Data”, IEEE Trans. on Semiconductor Manufacturing, Vol. 5, No 4, pp. 308-18, November 1992.
8. G. S. May and Costas J. Spanos, “Automated Malfunction Diagnosis of Semiconductor Fabrication Equipment: A Plasma Etch Application”, IEEE Trans. on Semiconductor Manufacturing, Vol. 6, No 1, pp. 28-40, February 1993.
9. E. Boskin, Costas J. Spanos, G. Korsh, “A Method for Modeling the Manufacturability of IC Designs”, IEEE Trans. on Semiconductor Manufacturing, Vol. 7, No 3, pp. 298-305, August 1994.
10. S. Lee and Costas J. Spanos, “RTSPC: A Software Utility for Real-Time SPC and Tool Data Analysis”, IEEE Trans. on Semiconductor Manufacturing, Vol. 8, No 1, pp. 17-25, February 1995.
11. C. Yu, T. Maung, Costas J. Spanos, D. Boning, J. Chung, H-Y Liu, K-J Chang and D. Bartelink, “Use of Short-Loop Electrical Measurements for Yield Improvement”, IEEE Trans. on Semiconductor Manufacturing, Vol. 8, No 2, pp. 150-159, May 1995.
12. S. Cunningham, Costas J. Spanos, K. Voros, “Semiconductor Yield Improvement: Results and Best Practices”, IEEE Trans. on Semiconductor Manufacturing, Vol. 8, No 2, pp. 103-109, May 1995.
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14. S. Leang and Costas J. Spanos, “A Novel In-line Automated Metrology for Photolithography”, IEEE Trans. on Semiconductor Manufacturing, Vol 9, No 1, pp. 101-7, February 1996.
15. Crid Yu, Costas J. Spanos, Hua Yu Liu and Dirk Bartelink, “Lithography Error Sources Quantified by Statistical Metrology”, Solid State Technology, February 1996.

16. S. Leang, S-Y Ma, J. Thomson, B. Bombay and Costas J. Spanos, "A Control System for Photolithographic Sequences", IEEE Trans. on Semiconductor Manufacturing, Vol 9, No 2, pp. 191-207, May 1996.
17. E. Palmer, W. Ren, Costas J. Spanos and K. Poolla, "Control of Photoresist Properties: A Kalman Filter Based Approach", IEEE Trans. on Semiconductor Manufacturing, Vol 9, No 2, pp. 208-14, May 1996.
18. Roawen Chen, Herb Huang, Costas J. Spanos, Michael Gatto, "Plasma Etch Modeling Using Optical Emission Spectroscopy", Journal of Vacuum Science Technology, A 14(3), May/ June 1996.
19. Antonio J. Miranda and Costas J. Spanos, "Impedance Modeling of a Cl₂/He Plasma Discharge", Journal of Vacuum Science Technology, A 14(3), May/June 1996.
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21. Costas J. Spanos and R. Chen, "Qualitative Modeling for Process Control in Semiconductor Manufacturing", IEEE Trans. on Semiconductor Manufacturing, Vol 10, No 2, pp. 307-16, May 1997.
22. S. Leang and Costas J. Spanos, "A General Equipment Diagnosis System and its Application on Photolithographic Sequences", IEEE Trans. on Semiconductor Manufacturing, Vol 10, No 3, pp. 329-43, August 1997 (Best Paper Award)
23. Zhihao Lin, Member, IEEE, Costas J. Spanos, Senior Member, IEEE, Linda S. Milor, Member, IEEE, and Y. T. Lin, "Circuit Sensitivity to Interconnect Variation", IEEE Trans. on Semiconductor Manufacturing, Vol. 11, No. 4, pp. 557-68, November 1998
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25. Mason Freed, Michiel Kruger, Costas J. Spanos and Kameshwar Poolla, "Autonomous on-wafer sensors for process modeling, diagnosis, and control", IEEE Trans. on Semiconductor Manufacturing, Vol. 14, No. 3, pp. 255-264, Aug, 2001.
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- microfield optic”, Journal of Vacuum Science Technology B, Vol. 24, No. 3, pp 1234-7, May/June 2006
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352. Zou, Han; Zhou, Yuxun; Yang, Jianfei; Gu, Weixi; Xie, Lihua; Spanos, Costas J; Wifi-based human identification via convex tensor shapelet learning Thirty-Second AAAI Conference on Artificial Intelligence 2018
353. Jin, Ming; Jia, Ruoxi; Das, Hari Prasanna; Feng, Wei; Spanos, Costas; Biscuit: Building intelligent system customer investment tools Proc. 10th International Conference on Applied Energy (ICAE) 2018
354. H Zou, J Yang, H Prasanna Das, H Liu, Y Zhou, CJ Spanos, WiFi and Vision Multimodal Learning for Accurate and Robust Device-Free Human Activity Recognition, Proceedings of

- The IEEE Conference on Computer Vision and Pattern Recognition (CVPR) Workshops, 2019, pp. 0-0
355. Zou, Han; Yang, Jianfei; Zhou, Yuxun and Spanos, Costas J, Joint Adversarial Domain Adaptation for Resilient WiFi-Enabled Device-Free Gesture Recognition, 2018 17th IEEE International Conference on Machine Learning and Applications (ICMLA), 202—207, 2018, IEEE
 356. Zou, Han; Zhou, Yuxun; Yang, Jianfei; Liu, Huihan; Das, Hari Prasanna and Spanos, Costas J, Consensus adversarial domain adaptation, Proceedings of the AAAI Conference on Artificial Intelligence 33, 5997—6004, 2019
 357. Zou, Han; Yang, Jianfei; Prasanna Das, Hari; Liu, Huihan; Zhou, Yuxun and Spanos, Costas J, WiFi and Vision Multimodal Learning for Accurate and Robust Device-Free Human Activity Recognition, Proceedings of the IEEE Conference on Computer Vision and Pattern Recognition Workshops, 2019
 358. Das, Hari Prasanna; Konstantakopoulos, Ioannis C; Manasawala, Aummul Baneen; Veeravalli, Tanya; Liu, Huihan; Spanos, Costas J; ,A novel graphical lasso based approach towards segmentation analysis in energy game-theoretic frameworks, 2019 18th IEEE International Conference On Machine Learning And Applications (ICMLA),1702-1709, 2019,IEEE
 359. Spangher, Lucas; Tawade, Akaash; Devonport, Alex; Spanos, Costas; ,Engineering vs. Ambient type visualizations: Quantifying effects of different data visualizations on energy consumption, Proceedings of the 1st ACM International Workshop on Urban Building Energy Sensing, Controls, Big Data Analysis, and Visualization,14-22, 2019
 360. Das, Hari Prasanna and Konstantakopoulos, Ioannis C and Manasawala, Aummul Baneen and Veeravalli, Tanya and Liu, Huihan and Spanos, Costas J, A novel graphical lasso based approach towards segmentation analysis in energy game-theoretic frameworks, 2019 18th IEEE International Conference On Machine Learning And Applications (ICMLA), 1702--1709, 2019, IEEE
 361. Periyakoil, Divya and Das, Hari Prasanna and Spanos, Costas J, Understanding Distributions of Environmental Parameters for Thermal Comfort Study in Singapore, Proceedings of the Eleventh ACM International Conference on Future Energy Systems, 461--465, 2020
 362. Spangher, Lucas and Gokul, Akash and Khattar, Manan and Palakapilly, Joseph and Tawade, Akaash and Bouyamourn, Adam and Devonport, Alex and Spanos, Costas,
 363. Prospective experiment for reinforcement learning on demand response in a social game framework, Proceedings of the Eleventh ACM International Conference on Future Energy Systems, 438--444, 2020
 364. Spangher, Lucas and Gokul, Akash and Khattar, Manan and Palakapilly, Joseph and Agwan, Utkarsha and Tawade, Akaash and Spanos, Costas, Augmenting Reinforcement Learning with a Planning Model for Optimizing Energy Demand Response, Proceedings of the 1st International Workshop on Reinforcement Learning for Energy Management in Buildings \& Cities, 39--42, 2020
 365. Chandra, Rohit and Thong, Hoan and Goh, Edwin and Panda, Sanjib Kumar and Spanos, Costas J and others, Demonstration of Transactive Control of Commercial Buildings as Energy Nodes, IECON 2020 The 46th Annual Conference of the IEEE Industrial Electronics Society, 1968--1973, 2020, IEEE
 366. Chandra, Rohit and Yadav, Gorla Naga Brahmendra and Subramaniam, Aravinth and Malik, Hasmat and Panda, Sanjib Kumar and Poolla, Kameshwar and Spanos, Costas J, A Survey of

Failure Mechanisms and Statistics for Critical Electrical Equipment in Buildings, IECON 2020 The 46th Annual Conference of the IEEE Industrial Electronics Society, 1955--1961, 2020, IEEE

367. Yang, Jianfei and Zou, Han and Xie, Lihua and Spanos, Costas J, Deep Learning and Unsupervised Domain Adaptation for WiFi-based Sensing, Generalization With Deep Learning: For Improvement On Sensing Capability, 79--100, 2021

Workshops, Tutorials, Invited Talks and Reports

368. Costas J. Spanos, "Process Characterization and Diagnosis", Third Annual SRC/DARPA, CIM-IC Workshop, Stanford University, August 1988.
369. Costas J. Spanos, "Equipment Diagnostics for Semiconductor Manufacturing", SPC Workshop, IEEE Symposium on VLSI Technology, Kyoto, Japan, May 1989.
370. N. H. Chang and Costas J. Spanos, "A CAM Framework and its Application for Monitoring and Diagnosis in VLSI Manufacturing", Fourth Annual SRC/DARPA CIM-IC Workshop, University of Michigan, August 1989.
371. K. K. Lin and Costas J. Spanos, "Statistical Equipment Modeling and Recipe Generation for VLSI Manufacturing", Fourth Annual SRC/DARPA CIM-IC Workshop, University of Michigan, August 1989.
372. Costas J. Spanos (editor), "Special Issues in Semiconductor Manufacturing - I", EECS, University of California at Berkeley, Memorandum No. UCB/ERL M90/8, January 1990.
373. Costas J. Spanos, "Statistical Process Control in Semiconductor Manufacturing", Short Course, University of California Extension School, San Francisco, CA, May 24-25 1990.
374. Costas J. Spanos, "Statistical Process Control in Semiconductor Manufacturing", Invited Tutorial, IMEC Summer Course in Manufacturing Science, Leuven Belgium, June 1990.
375. Costas J. Spanos, "Creating and Using Equipment Models in Semiconductor Manufacturing", Invited Tutorial, IMEC Summer Course in Manufacturing Science, Leuven Belgium, June 1990.
376. Costas J. Spanos, "Using Regression Equations for Model-Based Diagnosis in the Berkeley Computer-Aided Manufacturing System", Workshop on Intelligent Diagnostic and Control Systems for Manufacturing, AAI, Boston, MA, July 1990.
377. G. S. May and Costas J. Spanos, "Modeling and Diagnosis of a Plasma Etcher", Fifth Annual SRC/DARPA CIM-IC Workshop, Berkeley, CA, August 1990.
378. Z. M. Ling and Costas J. Spanos, "In-Line Supervisory Control in a Photolithography Workcell", Fifth Annual SRC/DARPA CIM-IC Workshop, Berkeley, CA, August 1990.
379. H. F. Guo and Costas J. Spanos, "Multivariate SPC of a Plasma Etcher", Fifth Annual SRC/DARPA CIM-IC Workshop, Berkeley, CA, August 1990.
380. Costas J. Spanos, "Statistical Process Control in Semiconductor Manufacturing", Microelectronic Engineering 10 (1991) pp. 271-276, Elsevier Science Publishers.
381. Costas J. Spanos, "Creating and Using Equipment Models in Semiconductor Manufacturing", Microelectronic Engineering 10 (1991) pp. 199-205, Elsevier Science Publishers.
382. Costas J. Spanos (editor), "Special Issues in Semiconductor Manufacturing - II", EECS, University of California at Berkeley, Memorandum No. UCB/ERL M91/8, January 1991.
383. Costas J. Spanos, "Issues in Real-Time Statistical Process Control", Invited Paper, presented at the 1991 SRC Workshop on real Time Controllers, Vancouver, February 19, 1991.

384. Costas J. Spanos, "What is Statistical Process Control?", 1991 International Semiconductor Manufacturing Sciences Symposium, Workshop on SPC, San Mateo, CA, May 21, 1991.
385. Costas J. Spanos, "Tool Control - Objectives for the year 2000 and beyond", White paper commissioned by SRC and Sematech, June 1991.
386. Costas J. Spanos, "Equipment and Process Control Issues", Sixth Annual SRC/DARPA CIM-IC Workshop, North Carolina State University, NC, August 1991
387. Costas J. Spanos, "The Berkeley Computer-Aided Manufacturing System", Sixth Annual SRC/ DARPA CIM-IC Workshop, North Carolina State University, NC, August 1991
388. S. Leang and Costas J. Spanos, "Statistically-Based feedback Control", Sixth Annual SRC/ DARPA CIM-IC Workshop, North Carolina State University, NC, August 1991.
389. S. Lee and Costas J. Spanos, "Rapid Development of Physically-Based Equipment Models", Sixth Annual SRC/DARPA CIM-IC Workshop, North Carolina State University, NC, August 1991.
390. E. Boskin and Costas J. Spanos, "Binning of Commodity ICs", Sixth Annual SRC/DARPA CIM- IC Workshop, North Carolina State University, NC, August 1991.
391. K. K. Lin and Costas J. Spanos, "Development and Applications of Equipment-Specific Process Models for Semiconductor Manufacturing", book chapter in Intelligent Modeling, Diagnosis and Control of Manufacturing Processes, by World Scientific Publishing 1992.
392. Costas J. Spanos (editor), "IC Design for Manufacturability", EECS, University of California at Berkeley, Memorandum No. UCB/ERL M92/17, February 1992.
393. Costas J. Spanos, "The Berkeley Computer-Aided Manufacturing System", Invited Talk, Sematech Process and Equipment Control Workshop, March 18, 1992.
394. Costas J. Spanos, "The Berkeley Computer-Aided Manufacturing System", Invited Talk, SRC Video Course, June 9, 1992.
395. Costas J. Spanos, "A Multi-Variate, Multi-Step Equipment Controller", Invited talk given at the DEC Technical Seminar Series in Hudson, MA, June 10, 1992.
396. Costas J. Spanos, "The Berkeley Real-Time Statistical Process Control Method", Invited talk given at IBM in Fishkill NY on June 11, 1992.
397. Costas J. Spanos, "Statistical Process Control in Semiconductor Manufacturing", 1992 International Semiconductor Manufacturing Sciences Symposium, Workshop on SPC, San Francisco, CA, June 17, 1992.
398. H-C Liu and Costas J. Spanos, "Automatic Time-Series Model Generation for Semiconductor Manufacturing", Seventh Annual SRC/DARPA CIM-IC Workshop, Stanford University, August 1992.
399. R. Chen and Costas J. Spanos, "Fuzzy Modeling of Semiconductor Processing Equipment", Seventh Annual SRC/DARPA CIM-IC Workshop, Stanford University, August 1992.
400. Costas J. Spanos, S. Leang and J. Thomson, "A Supervisory Controller for Semiconductor Manufacturing", Seventh Annual SRC/DARPA CIM-IC Workshop, Stanford University, August 1992.
401. Costas J. Spanos and L. Rowe, "The Berkeley CIM/CAM Research Program", Invited talk at the Seventh Annual SRC/DARPA CIM-IC Workshop, Stanford University, August 1992.
402. Costas J. Spanos (editor), "Special Issues in Semiconductor Manufacturing - III", EECS, University of California at Berkeley, Memorandum No. UCB/ERL M92/84, August 1992.
403. Costas J. Spanos, S. Leang and S. Lee, "A Control and Diagnosis Scheme for Semiconductor Manufacturing", Invited Paper to the American Control Conference, San Francisco, CA, June 1993.

404. Costas J. Spanos, "Research Directions in Semiconductor Manufacturing", Keynote Speech, Semiconductor Manufacturing Technology Workshop, Hsinchu, Taiwan, March 1993.
405. Costas J. Spanos, "Equipment Diagnosis", Semiconductor Manufacturing Technology Workshop, Hsinchu, Taiwan, March 1993.
406. Neureuther, Costas J. Spanos, M. Hatzilambrou and C. Yu, "Concurrent Circuit Design/ Process Engineering in a Flexible Manufacturing Environment", White Paper, EECS, University of California at Berkeley, Memorandum No. UCB/ERL M93/91, December 1993.
407. Costas J. Spanos (editor), "Special Issues in Semiconductor Manufacturing - IV", EECS, University of California at Berkeley, Memorandum No. UCB/ERL M94/2, February 1994.
408. Costas J. Spanos, S. Cunningham and L. Smith, "The Statistics of In-Situ particle Monitoring", Invited paper, presented at the meeting of the Electrochemical Society, May 1994.
409. J. Spanos, "Advance Process Identification Techniques", book chapter in Statistical Approach to VLSI Design, series in Advances in CAD for VLSI by North Holland Publishing Co, 1994.
410. Costas J. Spanos, "The Berkeley Computer-Aided Manufacturing System", invited talk presented at the VI AEC/APC Sematech Workshop, September 1994.
411. Costas J. Spanos, "The Intelligent Factory - Applying Process Control in Semiconductor Manufacturing", invited talk, presented at the Korean Automatic Control Conference, October 1994, also at DEC Technical Seminar Series and Arizona State University, November 1994.
412. Costas J. Spanos, Sherry Lee, Roawen Chen, Tony Miranda, Sundeep Rangan and Herb Huang, "From Open Loop to Run-to-run and Real-time Control for Plasma Processes", invited talk, presented at the 3rd International Workshop on Advanced Plasma Tools, May 3, 1995.
413. Costas J. Spanos and Shang-Yi Ma, "A Multistep Supervisory Controller for Photolithographic Operations", invited talk at the 187th ECS Meeting, 1st Symposium on Process Control, Diagnostics and Modeling in Semiconductor Manufacturing, Reno, May 21-26, 1995.
414. R. L. Chen and Costas J. Spanos, "Fuzzy Inference System For Semiconductor Manufacturing Processes", invited paper in the Proceeding of Applications of Fuzzy Logic Technology II, SPIE 1995 Symposium on OE/Aerospace Sensing and Dual Use Photonics, 17-21 April 1995, Orlando, Florida.
415. Costas J. Spanos (editor), "Special Issues in Semiconductor Manufacturing - V", EECS, University of California at Berkeley, Memorandum No. UCB/ERL M95/63, August 1995.
416. Costas J. Spanos (editor), "Special Issues in Semiconductor Manufacturing - VI", EECS, University of California at Berkeley, Memorandum No. UCB/ERL M95/64, August 1995.
417. Costas J. Spanos, "The Intelligent IC Factory", 32 min video tape made by the Semiconductor Research Corporation, September 1995.
418. Costas J. Spanos, "Real-time plasma modeling and Control", invited talk presented at the VII AEC/APC Sematech Workshop, October 1995.
419. Costas J. Spanos, "Fault Detection and Process Control under Development in the University Community - What is Possible in the Future?", invited talk at the 1996 Manufacturing Science and Technology Group technical sessions at AVS, October 1996.
420. Costas J. Spanos, "Advanced Process Control - Does it belong in IC Production?", invited tutorial presented at the 6th AEC/APC Workshop, given by Sematech, October 1996.
421. Costas J. Spanos, "The Next Generation Photolithography Control", Professional Lithography Workshop, Belgium, October 1997.
422. Costas J. Spanos, "Advanced Lithography Control", short course given at SPIE's 23rd Annual International Symposium on Microlithography, February 1998.

423. Costas J. Spanos, Panel Discussion Integrated Metrology: Effective Hardware and Control Strategies, SPIE 2003.
424. Costas J. Spanos, "APC Landscape in the Semiconductor Industry", Keynote, Intel Semiconductor Manufacturing Conference, Phoenix, AZ, March 2003
425. Costas J. Spanos, "Some Thoughts on Integrated Metrology & Control", Panel Discussion, Intel APC Summit, Albuquerque NM, March 2004
426. Costas J. Spanos, "Coping with Variability in Semiconductor Manufacturing", Invited Paper, Modeling and Control for Microelectronics Manufacturing (Invited Session), American Institute of Chemical Engineers, 2004 Annual Meeting, Austin, Texas, November 2004
427. Costas J. Spanos, "Advanced Process Control Landscape in the Semiconductor Industry", Invited Panelist to Intel Corporation's AEC/APC conference on March 2005,
428. Costas J. Spanos, "Advanced Process Control Landscape in the Semiconductor Industry", KLA Webcast, March 2005
429. Paul Friedberg, Willy Cheung, and Costas J. Spanos, "Spatial Variability of Critical Dimensions," VLSI/ULSI Multilevel Interconnection Conference XXII, pp. 539-546, Sept 2005.
430. Costas J. Spanos and Tom Sonderman, "Advanced Process Control in Semiconductor Manufacturing", WebCast by the American Institute of Chemical Engineers, 10/28/2005.
431. Costas J. Spanos, "Metrology in the DFM Era", Invited Keynote to Timbre/TEL user's forum, February 26, 2007, San Jose, CA.
432. Mei Sun and Costas J. Spanos, "Wafer-based Metrology Systems", Invited Keynote to KLA-Tencor Inventions Luncheon, March 8, 2007, Santa Clara, CA.
433. Costas J. Spanos, "Opportunities in Semiconductor Manufacturing", CITRIS Asia Taipei & HsinChu, Taiwan, March 27-28, 2007.
434. Jing Xue and Costas J. Spanos, "An Integrated Aerial Image Sensor for Lithography Diagnostics", International Workshop on Electron Devices and Semiconductor Technology (IEDST 2007) June 3-4, 2007, Tsinghua University, Beijing, China
435. Invited Panelist on Design for Manufacturability discussion at the 2008 SPIE conference (Society of Photo-Optical Instrumentation Engineers), February 2008.
436. Invited Presenter at the CITRIS-Copenhagen Research Conference on Climate and Energy, June 19-20, 2008.
437. Costas J. Spanos, "Needed Innovations at the Design-Manufacturing Interface", Invited Talk, CITRIS Exchange, November 14th, 2007.
438. Costas J. Spanos, "Design for Manufacturability of State of the Art Integrated Circuits", Invited Talk, July 11th, 2008, University of Science Technology of China, Hefei, China.
439. Costas J. Spanos, "Modelling IC Variability for Process-Design Co-Optimization", Invited Talk, Semiconductor Research Corporation, e-Workshop, September 24th, 2008.
440. Sam Sivakumar, Tim Brunner and Costas J. Spanos, "Concerning the obvious superiority of MfD over DfM", Invited Panel, SPIE, San Jose, CA, February 25th 2009.
441. Costas J. Spanos, "Can IT Innovation Solve the Energy Challenge? Buildings, Distribution, Computing", Invited Talk at Google, May 5 2009
442. Costas J. Spanos, "Building Energy Systems", Invited talk at CITRIS-Siemens conference, Munich, Germany, May 28, 2009.
443. Costas J. Spanos, "Energy Efficiency in Buildings", Short course at the Haas School of Business, UC Berkeley, CA, August 18th, 2009.
444. Costas J. Spanos, "IC Variability – An Overview", IMPACT Seminar, November 18th, 2009.

445. Costas J. Spanos, “Connected Buildings: Energy Efficiency, Demand/ Response, and ICT”, invited talk, Changua Leadership Institute in collaboration with CISCO, Berkeley, CA, May 12, 2010.
446. Costas J. Spanos, “Statistical Description of Process Variability”, First International Variability Characterization Workshop, Hsinchu, Taiwan, April 30th, 2010.
447. Costas J. Spanos, “Reducing Data Centers’ Environmental Footprint Without Compromising Performance and Competitiveness”, Invited Talk, International Green energy Forum, Shanghai, China, June 18-20, 2010.
448. Costas J. Spanos, “A Roadmap towards Highly Efficient Buildings”, 2nd Tsinghua - UCB Forum for Green Electronics and Buildings, Beijing, June 22nd, 2010.
449. Costas J. Spanos, “Design for Manufacturability of State of the Art Integrated Circuits”, Invited Seminar, Corallia, Athens, Greece, June 30th, 2010.
450. Costas J. Spanos, “The Self-Optimizing Building”, Invited talk at Hong Kong University, December 17th, 2010.
451. Costas J. Spanos, “Integrated Circuit Variability”, Invited Talk at Hong Kong University of Science and Technology, December 20th, 2010.
452. Costas J. Spanos, “Buildings and Energy”, Invited Dinner Talk, LoCal Retreat., Tahoe, CA, January 13th, 2011.
453. Costas J. Spanos, “Some thoughts on Electricity and its Engineering”, Invited Panel Discussion at the Electrical and Computer Engineering Department Heads Association Meeting, Phoenix, AZ, March 14th, 2011.
454. Costas J. Spanos, “The Self-Optimizing Building”, Tsinghua University, Beijing, China, March 23rd 2011.
455. Costas J. Spanos, “Technology Transfer Stories”. Invited Talk at the National Academies Board on Science, Technology, and Economic Policy, Palo Alto, CA, October 27th, 2011.
456. Costas J. Spanos, “Capturing, Modeling and Leveraging Process Variability in IC Design, Invited Keynote at the Design Technologies Workshop, École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland, January 19th, 2012.
457. Costas J. Spanos, “Leveraging Variability in Design, Manufacturing and Energy Sustainability”, invited Talk, Singapore University of Technology and Design, Singapore, July 3rd, 2012.
458. Costas J. Spanos, “The Agile Building”, Invited Keynote, 2nd International Conference on Building Energy and Environment, Boulder, Colorado, August 2nd, 2012.
459. Costas J. Spanos, “Capturing and Leveraging Process Variability”, Invited Talk, Nanometrics, October 2nd, 2012.
460. Costas J. Spanos, “The Realities of Virtual Metrology”, Invited Talk, International Symposium on Semiconductor Manufacturing, Tokyo, Japan, October 17th, 2012.
461. Costas J. Spanos, “Capturing, Modeling and Leveraging Process Variability in IC Design”, Invited Talk, Carnegie Mellon University, March 28th, 2013.
462. Costas J. Spanos, “Building Efficiency and Sustainability in the Tropics”, Invited Talk, International Green Building Conference, Singapore, September 12th, 2013.
463. Costas J. Spanos, “Building Efficiency and Sustainability in the Tropics”, Invited Talk, ETH Zurich, March 6th, 2014.
464. Pushkar P. Apte, Costas J. Spanos, Masayoshi Tomizuka, Edwin Goh and SinBerBEST Team, “Integrated Cyber-Physical Test bed to Optimize Energy Efficiency & Human Comfort in Buildings”, Invited Workshop, CASE 2015.

465. Costas J. Spanos, “Building Energy Efficiency and Sustainability in the Tropics”, Invited Talk, Tsinghua-Berkeley Schengen institute, Invited Talk, November 3rd, 2015
466. Costas J. Spanos, “Exponentials, Sigmoids, and Inventing the New Wheel”, QTECH 2016 (Qualcomm Invited keynote), June 29, 2016
467. Costas J. Spanos, “Building the Brave New World”, BECA Asia leadership Conference 2016. Invited keynote, Singapore, August 2nd, 2016
468. Costas J. Spanos, Yuxun Zhou, Ming Jin, Ruoxi Jia, Zhanbo Xu, Han Zou, Ioannis Konstantakopoulos, Dan Li, Weixi Gu, Hu Guojang, “Smart Buildings as Cyber-Physical Systems: Statistical Learning, Control and Automatic Design”, SmartGridComm, Sydney, November 6, 2016
469. Costas J. Spanos, “How to trim 10 Terawatts of Electricity - Smart buildings in the Tropics”, Invited talk, Building Energy Efficiency Workshop, CDC, Las Vegas, December 11, 2016
470. Costas J. Spanos, “The Next IT Revolution”, Executive Education Lecture for ENEL, UC Berkeley, May 10, 2017.
471. Costas J. Spanos, “Exponentials, Sigmoids, and Imagining and New IT Revolution”, Nanyang Technological university, Singapore, Invited Lecture, May 26, 2017.
472. Costas J. Spanos, “Innovation for Industry, CITRIS and the Banatao Institute”, Inclusive Innovation Conference 2017, Invited keynote, Manilla, Philippines, May 30, 2017
473. Costas J. Spanos, “Designing Curriculum for A.I.”, Inclusive Innovation Conference 2017, Invited keynote, Manilla, Philippines, May 30, 2017
474. Costas J. Spanos, “Academe – Industry Linkages: CITRIS & the Banatao Institute”,
475. Costas J. Spanos, “Exponentials, Sigmoids, and Inventing the New Wheel”, Samsung Speaker Series, June 27, 2017
476. Wang, Jingkan; Jia, Ruoxi; Friedland, Gerald; Li, Bo; Spanos, Costas; One Bit Matters: Understanding Adversarial Examples as the Abuse of Redundancy arXiv preprint arXiv:1810.09650 2018
477. Das, Hari Prasanna; Konstantakopoulos, Ioannis C; Manasawala, Aummul Baneen; Veeravalli, Tanya; Liu, Huihan; Spanos, Costas J; “Segmentation Analysis in Human Centric Cyber-Physical Systems using Graphical Lasso”, arXiv preprint arXiv:1810.10533 2018
478. Konstantakopoulos, Ioannis C; Barkan, Andrew R; He, Shiyang; Veeravalli, Tanya; Liu, Huihan; Spanos, Costas; A deep learning and gamification approach to energy conservation at Nanyang Technological University arXiv preprint arXiv:1809.05142 2018
479. Costas J. Spanos “Exponentials, Sigmoids, & Inventing the New Wheel (CITRIS and our work in Singapore)”, Invited Lecture, Hong Kong University of Science and Technology, January 9, 2018
480. Costas J. Spanos “Exponentials, Sigmoids, & Inventing the New Wheel (CITRIS and our work in Singapore)”, Invited Lecture, Tsinghua University, January 12, 2018
481. Costas J. Spanos “Future Impact of Transformative Technologies”, Invited Lecture, SEMI CTO Forum, June 13, 2018
482. Han Zhou and Costas J. Spanos “Mining Information from Passive RF Sensing of IoT Networks”, NSF IoT Workshop, San Diego, November 4, 2018
483. Costas J. Spanos “Designing a Living Laboratory for Building Energy Efficiency in the Tropics”, Invited talk, Building Energy Efficiency Workshop, CDC, Miami, December 16, 2018
484. Das, Hari Prasanna and Konstantakopoulos, Ioannis C and Manasawala, Aummul Baneen and Veeravalli, Tanya and Liu, Huihan and Spanos, Costas J, Segmentation Analysis in Human

- Centric Cyber-Physical Systems using Graphical Lasso, arXiv preprint arXiv:1810.10533, 2019
485. Yang, Yu and Hu, Guoqiang and Spanos, Costas J, HVAC Energy Cost Optimization for a Multi-zone Building via a Decentralized Approach, arXiv preprint arXiv:1905.10934, 2019
 486. Das, Hari Prasanna and Abbeel, Pieter and Spanos, Costas J, Dimensionality Reduction Flows, arXiv preprint arXiv:1908.01686, 2019
 487. Jia, Ruoxi and Dao, David and Wang, Boxin and Hubis, Frances Ann and Gurel, Nezihe Merve and Li, Bo and Zhang, Ce and Spanos, Costas J and Song, Dawn, Efficient Task-Specific Data Valuation for Nearest Neighbor Algorithms, arXiv preprint arXiv:1908.08619, 2019
 488. Costas J. Spanos “Harnessing the Next Revolution”, Invited Lecture, Lam Research, January 14, 2019
 489. Costas J. Spanos “Smart Energy”, International Workshop on Applied Machine Learning for Intelligent Energy Systems, June 25, 2019
 490. Costas J. Spanos “Harnessing the Smart Energy Revolution”, invited Seminar, Nanyang Technological University, Singapore, August 13, 2019
 491. Das, Hari Prasanna; Abbeel, Pieter; Spanos, Costas J; ,Dimensionality reduction flows, arXiv preprint arXiv:1908.01686, 2019
 492. Jia, Ruoxi; Dao, David; Wang, Boxin; Hubis, Frances Ann; Gurel, Nezihe Merve; Li, Bo; Zhang, Ce; Spanos, Costas J; Song, Dawn; ,Efficient task-specific data valuation for nearest neighbor algorithms, arXiv preprint arXiv:1908.08619, 2019
 493. Yang, Yu; Hu, Guoqiang; Spanos, Costas J; ,A Proximal Linearization-based Decentralized Method for Nonconvex Problems with Nonlinear Constraints, arXiv preprint arXiv:2001.00767, 2020
 494. Konstantakopoulos, Ioannis C; Hamilton, Kristy A; Veeravalli, Tanya; Spanos, Costas; Dong, Roy; smartSDH: A Mechanism Design Approach to Building Control, arXiv preprint arXiv:2001.02807, 2020
 495. Prasanna Das, Hari; Konstantakopoulos, Ioannis C; Baneen Manasawala, Aummul; Veeravalli, Tanya; Liu, Huihan; Spanos, Costas J; ,A Novel Graphical Lasso based approach towards Segmentation Analysis in Energy Game-Theoretic Frameworks, arXiv, arXiv: 1910.02217, 2019
 496. Konstantakopoulos, Ioannis C; Das, Hari Prasanna; Barkan, Andrew R; He, Shiyang; Veeravalli, Tanya; Liu, Huihan; Manasawala, Aummul Baneen; Lin, Yu-Wen; Spanos, Costas J; ,Design, benchmarking and explainability analysis of a game-theoretic framework towards energy efficiency in smart infrastructure, arXiv preprint arXiv:1910.07899, 2019,
 497. Yang, Yu; Hu, Guoqiang; Spanos, Costas J; ,Stochastic Optimal Control of HVAC system for Energy-efficient Buildings, arXiv preprint arXiv:1911.00840, 2019,
 498. Yang, Yu and Hu, Guoqiang and Spanos, Costas J, A Proximal Linearization-based Decentralized Method for Nonconvex Problems with Nonlinear Constraints, arXiv preprint arXiv:2001.00767, 2020
 499. Konstantakopoulos, Ioannis C and Hamilton, Kristy A and Murthy, Yashaswini and Veeravalli, Tanya and Spanos, Costas and Dong, Roy, smartSDH: A Mechanism Design Approach to Building Control, arXiv preprint arXiv:2001.02807, 2020
 500. Yang, Yu and Hu, Guoqiang and Spanos, Costas J, Optimal Sharing and Fair Cost Allocation of Community Energy Storage, arXiv preprint arXiv:2010.15455, 2020

501. Yang, Yu and Agwan, Utkarsha and Hu, Guoqiang and Spanos, Costas J, Selling Renewable Utilization Service to Consumers via Cloud Energy Storage, arXiv preprint arXiv:2012.14650, 2020

Issued US Patents

1. 9,029,728, “Methods of and apparatuses for measuring electrical parameters of a plasma process”
2. 8,698,037, “Methods of and apparatuses for maintenance, diagnosis, and optimization of processes”
3. 7,960,670, “Methods of and apparatuses for measuring electrical parameters of a plasma process”
4. 7,580,767, “Methods of and apparatuses for maintenance, diagnosis, and optimization of processes”
5. 7,531,984, “Sensor apparatus power transfer, communication and maintenance methods and apparatus”
6. 7,403,834, “Methods of and apparatuses for controlling process profiles”
7. 7,299,148, “Methods and apparatus for low distortion parameter measurements”
8. 7,282,889, “Maintenance unit for a sensor apparatus”
9. 7,016,754, “Methods of and apparatus for controlling process profiles”
10. 6,741,945, “Sensor geometry correction methods and apparatus”
11. 6,738,722, “Data collection and correction methods and apparatus”
12. 6,691,068, “Methods and apparatus for obtaining data for process operation, optimization, monitoring, and control”